REMARKS

Claims 23, 25-32 and 34 were pending in the present application. By way of the present amendment, claims 23, 31 and 32 have been amended, and new claims 35-39 have been added. Therefore, claims 23, 25-32 and 34-39 are presented for further consideration.

In the Office Action mailed May 27, 1997, claim 32 was noted as having an informality. By way of the present amendment, this informality has been corrected.

Claims 23, 25-26, 28-29 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chang; and claims 27, 30, 32 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chang in view of Jamoua. These rejections, to the extent that the PTO may apply them to the presently pending claims, are traversed for the reasons given below.

Independent claims 23 and 31 have been amended to recite a master processor, in which each of the signal processors notifies the master processor that it has written new data into the respective memory location where it is only allowed to write data. Thus, the master processor can obtain newly-written-in data from a plurality of memories that are being written into by a plurality of signal processors, respectively.

New claim 35 recites the signals used to notify the master processor of newly-written-in data; new claims 36 and 38 recite that the master processor has read and write access to all of the memories; and new claims 37 and 39 recite that the master processor always controls the slave processors.

These features are absent from the teachings of Chang and Jamoua. Chang discloses a Central Processor (CP) in Figure 3, as well as an interrupt system for providing communications between the CP and the modular processors (MPs). See page 2, second column of Chang. Chang also discloses that one result of the communications between processors is that "processors which share program memory (for example, p1, p2, p3, and MA) can

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execute the same routine or different routines simultaneously from the program memory." See page 2, second column, lines 25-27 of Chang. Thus, Chang's CP is different from claimed master processor, which utilizes the newly-written-in data by the signal processors to perform a task.

In contrast to the invention claimed herein, Chang's CP is used to handle "I/O to the main memories", as disclosed on page 2, second column of Chang. Still further, Chang's CP can be interrupted by any of the modular processors, thereby placing the CP at the same level as the modular processors. In other words, Chang's CP is not a "master" processor, since a master processor does not allow a slave processor to take over control of the master processor at any time. While a slave processor can provide a signal to the master processor to inform the master processor of an event (such as newly-written-in data to a memory), this is different from transferring control of the CP to an assigned address in the memory module of the interrupting modular processor, as is disclosed in page 2, column 2 of Chang. There is no suggestion in Chang of the first and second signals from the signal processors notifying a master processor of the presence of newly written data, as claimed herein.

Jamoua is used in the Office Action to disclose the use of multiple processors to control a servo loop function, and does not make up for the deficiencies of Chang, as discussed above.

Therefore, it is respectfully requested that the 35 U.S.C. § 102(b) and § 103(a) rejections of the claims be reconsidered and withdrawn.

For the aforementioned reasons, the application is considered to be in condition for allowance, and an early indication of allowance is earnestly solicited.

If there are any remaining issues that need to be addressed, the Examiner is encouraged to contact the undersigned at the local telephone exchange listed below.

Respectfully submitted,

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Date

for / Phillip J. Articola
Brian J. McNamara
Reg. No. 32,789

Reg. No. 38,819

FOLEY & LARDNER
Suite 500
3000 K Street, N.W.
Washington, DC 20007-5109
(202) 672-5300